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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/642,244
Filing Date: August 18, 2003
Appellant(s): LAI ET AL.

Joe McKinney Muncy
32,334
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 23, 2006 appealing from the Office action mailed July 25, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal..

The statement of the status of claims contained in the brief is correct.

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

The summary of claimed subject matter contained in the brief is correct.

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

The copy of the appealed claims contained in the Appendix to the brief is correct.

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson, U.S. Patent 6,525,953 B1.

3. Johnson discloses a semiconductor device as claimed. See **FIGS. 1-17**, where Johnson teaches the claimed invention.

4. Pertaining to claim 1, Johnson teaches a mask read only memory containing diodes, comprising:

a semiconductor substrate **100**;

an insulating layer **102** on the semiconductor substrate;

a plurality of first conductive lines **114** along a first direction on the insulating layer;

a plurality of vertical diodes **12** on the first conductive lines;

a plurality of dielectric layers **120** on part of the diodes; and

a plurality of second conductive lines **123/128** along a second direction on the dielectric layers and the diodes, wherein the first direction is perpendicular to the second direction.

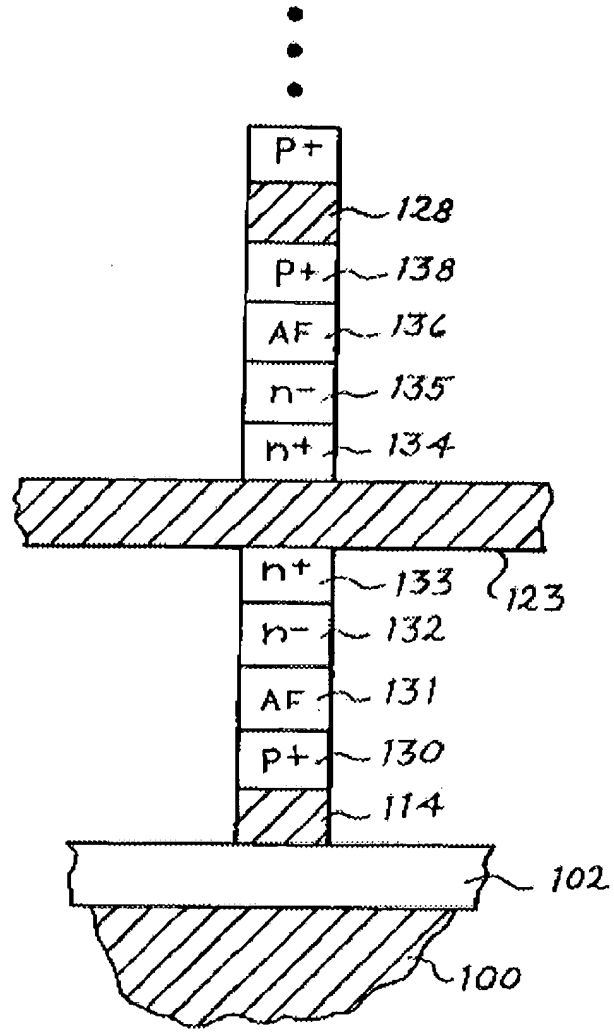


Fig. 7

5. Pertaining to claim 2, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the diodes are PN diodes.

6. Pertaining to claim 3, Johnson teaches the mask read only memory containing diodes as claimed in claim 2, wherein the PN diodes comprise two polysilicon layers of opposing conductive types.

7. Pertaining to claim 4, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the insulating layer is silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5) , barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2) .

8. Pertaining to claim 5, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the first conductive lines are bit lines and the second conductive lines are word lines (column 4, lines 60-63).

9. Pertaining to claim 6, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the dielectric layers are silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4) , tantalum pentoxide (Ta_2O_5) , barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2) .

10. Pertaining to claim 7, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, comprising: a semiconductor substrate;

an insulating layer on the semiconductor substrate; and

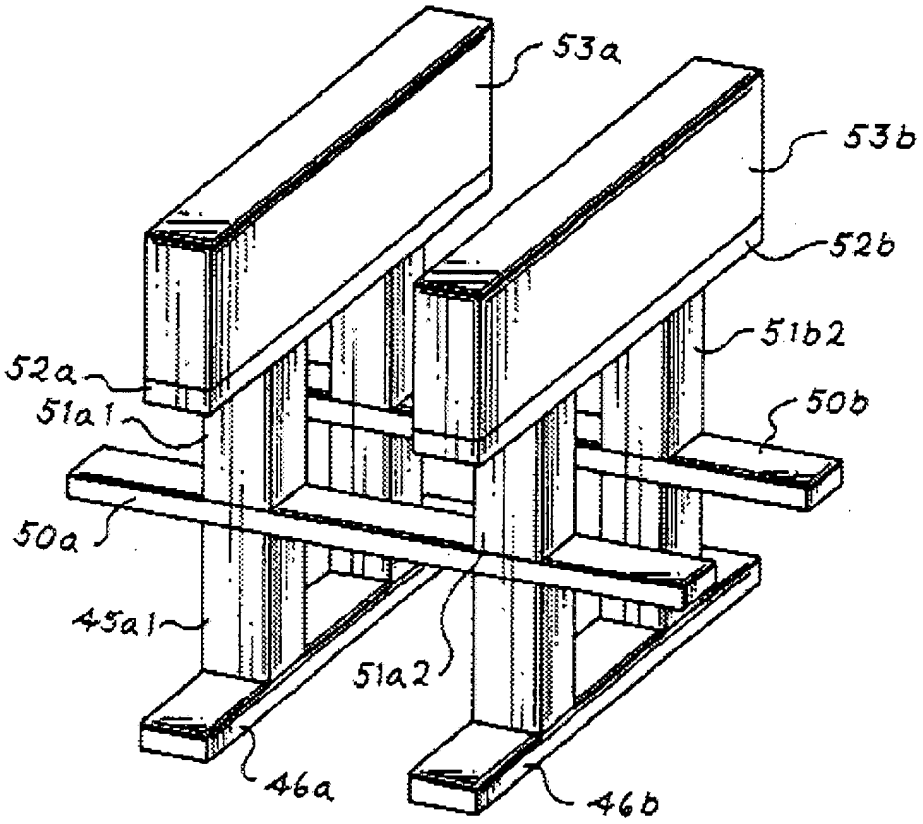
at least two memory cell layers stacked on the insulating layer wherein there is a separating layer between any two memory cell layers to provide insulation and wherein each memory cell layer comprises:

a plurality of first conductive lines along a first direction on the insulating layer;

a plurality of vertical diodes on the first conductive lines; a plurality of dielectric layers on part of the diodes; and a plurality of second conductive lines along a second direction on the dielectric layers and the diodes, wherein the first direction is perpendicular to the second

direction, wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides thereof of opposing conductive type face each other.

Fig. 10(f)



11. Pertaining to claim 8, Johnson teaches the mask read only memory containing diodes as claimed in claim 7, which comprises 2 to 10 memory cell layers.

12. Pertaining to claim 9, Johnson teaches the mask read only memory containing diodes as claimed in claim 7, wherein the separating layer is silicon dioxide, aluminum oxide ($A1_2O_3$), silicon nitride (Si_3N_4) , tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2) .

13. Pertaining to claim 10, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate;

n diode layers stacked on the insulating layer, wherein n is an integer equal to or greater than 2 and each diode layer comprises a plurality of vertical diodes and a plurality of dielectric layers on part of the diodes; and

(n + 1) parallel conductive layers disposed between the bottom diode layer and the insulating layer, on the top diode layer, and between any

two adjacent diode layers respectively, wherein the (n + 1) parallel conductive layers are disposed so that any two adjacent conductive layers are perpendicular to each other, wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides of matching conductive type face each other (also see column 7, lines 35-53).

14. Pertaining to claim11, Johnson teaches the mask read only memory containing diodes as claimed in claim 10, wherein n is between 2 and 10.

15. Pertaining to claim 20, Johnson teaches a mask read only memory containing diodes, comprising:

a semiconductor substrate;

an insulting layer on the semiconductor substrate;

a plurality of first conductive lines along a first direction on the insulating layer;

first and second vertical diodes on the first conductive lines;

a plurality of dielectric layers directly on the diodes (the Examiner takes the position that the phrase "subsequent dielectric depositions" is plural meaning more than one); and

a plurality of second conductive lines along a second direction directly on the dielectric layers and the second vertical diodes, wherein the first direction is perpendicular to the second direction.

(10) Response to Argument

Although the numeral 20 was missing in the heading of rejection on page 2, claim 20 is listed as being rejected on page 1 of the Final Office Action and clearly listed as rejected on page 7 and therefore Applicants argument is moot.

Applicants contend that the rejection of claims 1-11 and 20 under 35 U.S.C. § 102(e) is improper because the Examiner directs the Applicants to the background section of Johnson, U.S. Patent 6,525,953 herein known as Johnson. Specifically, Applicants argue that the dielectric layer on the diodes (i.e., pn junctions) as specified in claim 1 is not disclosed in Johnson because Applicants contend that the background is not part of the disclosure and relies on another reference.

Applicants claim 1 recites a plurality of dielectric layers on the diodes. The Johnson reference teaches the plurality of dielectric layers by showing dielectric layer **AF** in **FIG. 4** as being in several locations (i.e., anti-fuse material from a material such as silicon dioxide as disclosed in column 8, lines 61-64, please note that the anti-fuse material is a dielectric material). Additional

layers of dielectric are disclosed in column 9, lines 15-20 as to provide a dielectric between adjacent strips.

The insulator material is in physical contact with the diode columns and therefore on the pillars as disclosed above.

Applicants contend that Johns fails to teach a list of materials in claims 4, 6 and 9. However, the claim limitation does not required all of the materials to be present in the invention. The claims only indicate that only one of the materials have to be disclosed to meet the limitations of claims 4, 6 and 9. Because silicon dioxide is listed as one of the materials, Johns teaches Applicants claimed invention and therefore this argument is moot.

With regards to the rejection under the Japanese Patent Abstract Publication JP 06-334139 in which Applicants submitted with no explanation as to how the Japanese reference pertains to the patentability of the claims. Applicants provide no clear distinction of the rejection and the claimed limitations in the arguments filed July 11, 2005. However to expedite the Application the Examiner has dropped the rejection pertaining to Japanese Patent Abstract Publication 06-334139.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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